P0453

RAN-2403000502049005

RAN-2403000502049005

F. Y. B. Sc. (NCF- NEP) (Sem.-II) Examination October - 2025

ELEC-MDC Combinational Circuit Design Theory

સૂચના : / Instructions

(૧) નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fill up strictly the details of ☛ signs on your answer book

Name of the Examination:

☛ **F. Y. B. Sc. (NCF- NEP) (Sem.-II)**

Name of the Subject :

☛ **ELEC-MDC Combinational Circuit Design Theory**

Subject Code No.: **2403000502049005**

Seat No.:

Student's Signature

I. One word or short answer (Any 5) (5)

1. What is a Latch?
2. Give the Full form of K-map?
3. Draw the diagram of T Flip-flop?
4. Define Half adder.
5. What is a Register?
6. What do you mean by Synchronous Counter?

II. Answer (any 2) (10)

1. Draw the K- maps for 2 variable, 3 Variables and four variables and discuss the rule to minimize the Boolean function.
2. Minimize the Boolean function F(A, B, C, D) = ∑m(0, 1, 3, 5, 7, 8, 9, 11,13,15)
3. What is Combinational circuit? Design Half Subtractor.

III. Answer (any 2) (10)

1. Explain SOP and POS with respect to K maps?
2. Draw and explain 4-bit binary ripple counter.
3. Enlist types of flip-flops and explain briefly J K flip-flop